Conic display generator using multiplying digital-analog decoders

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INTRODUCTION

The need has been recognized for a computer-driven generator which is capable of drawing complex curves *without* imposing a great burden on the central computer. It has been shown that analog[1] and hybrid techniques[2,3] offer promise of lifting some of this computational and storage load. Past approaches using these techniques have been limited in speed and in kinds of curves drawn. Roberts has proposed a hybrid analog-digital generator based on homogeneous coordinate mathematics[4,5]. Such a generator has been designed and built using the wideband multiplying decoder as its basic component.[6]

General two-dimensional conic sections are drawn by this generator by the artifice of generating parabolic curves in 3-space and dividing by one of the coordinates to effect a perspective transformation onto a plane parallel to the plane of the remaining coordinates which becomes the plane of the display. Circles, ellipses, and hyperbolas are perspective transformations of the parabola. The 3-space vector generated parametrically as a function of time is:

$$\bar{p} = [x(t), y(t), w(t)] \tag{1}$$

where:

$$\begin{aligned} x(t) &= x_0 + x_1 t + x_2 t^2 \\ y(t) &= y_0 + y_1 t + y_2 t^2 \\ w(t) &= w_0 + w_1 t + w_2 t^2 \end{aligned} \tag{2}$$

Division by w(t) yields the vector

$$v = \left[\frac{x(t)}{w(t)}, \frac{y(t)}{w(t)}, 1 \right] \tag{3}$$

The direction of the vector remains unchanged by the division since all components are divided by the same quantity. The tip of the vector, however, lies on the plane w = 1. Fig. 1 illustrates this for a semicircle. The system described below is a hybrid analog-digital device which accomplishes the operations indicated in Eqs. 2 and 3.

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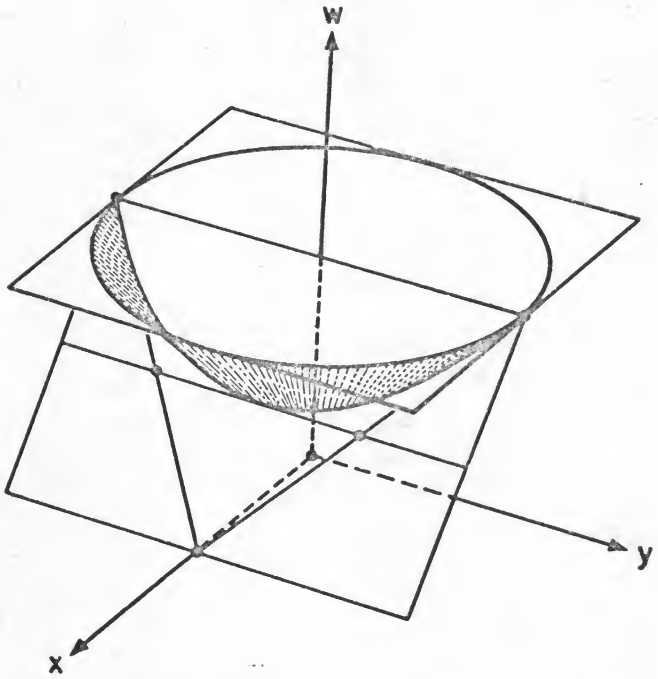

Figure 1—Projection of parabola into a circle in a homogeneous coordinate system

Operation of The Conic Generator

A block diagram of the system is shown in Figure 2. The blocks labeled t, w_0, w_2, x_1, x_2, etc, are multiplying decoders each of which produces an output equal to the product of analog voltage and a 10-bit digital number.* The multplying decoders are described in detail below (Figure 6 is the decoder schematic. The digital input for each decoder is held in a 10-bit buffer. The register holding the digital input for the two t-decoders is a 10-bit binary counter. To draw a curve segment the buffer registers holding the constants for the de-

coders (except the t-decoders) are filled by data transfers from the central computer. These are held constant for the duration of the segment. The t counter counts from 0 to 2^n ($O \leqq n < 10$) during a segment with the final count under program control. The t decoders are scaled so that the analog input voltages r and rt are multiplied by t ($0 \leqq t < 1$) over the counting range from 0 to 2^{10}. The frequency of the counter clock together with the total count determines the time to draw a segment. At the completion of a segment the counter is cleared. The buffers holding the constants, however, are not. For the next segment only those constants which have to be changed are affected.

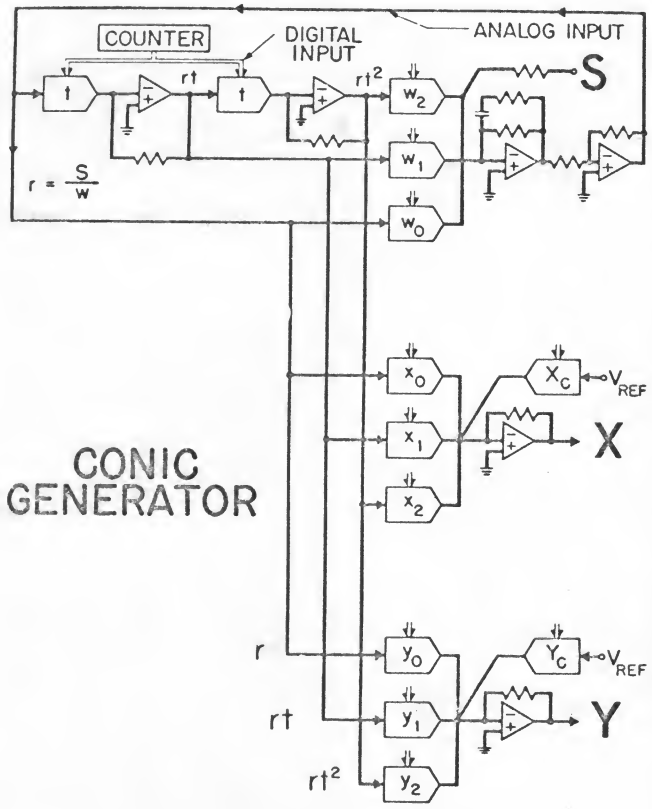

Figure 2—Conic generator block schematic

Consider the closed loop portion of the system. The effect of the high gain amplifier in the closed loop is to force the product of the analog voltage r and the digital number $w_0 + w_1t + w_2t^2$ to equal S. Or:

$$r = \frac{S}{w_0 + w_1t + w_2t^2} \tag{4}$$

Division by a second degree polynominal in the parameter t is thus accomplished. The analog signals r, rt, rt^2 so developed are multiplied by the digital numbers x_0, x_1, x_2, y_0, y_1, y_2 and translation constants Xc and Yc added to form the deflection signals.**

$$X = \frac{x(t)}{w(t)} + Xc = \frac{x_0 + x_1t + x_2t^2}{w_0 + w_1t + w_2t^2} + Xc$$
$$Y = \frac{y(t)}{w(t)} + Yc = \frac{y_0 + y_1t + y_2t^2}{w_0 + w_1t + w_2t^2} + Yc \tag{5}$$

A programming algorithm has been developed to determine the above coefficients. The range of w(t) is limited at the low end by the maximum output voltage of the amplifiers to +0.19. The range of w(t) during the drawing of a transformed conic determines how much of the conic may be drawn in one segment. For the limiting case of no variation in w where $w(t) = w_0$ (no time varying feedback) only straight lines and parabolas could be drawn. The other conics (as well as any other curves) would have to be pieced together with parabolic segments.

Two examples of conics generated by this display are shown in Figures 3 and 4. The circle was drawn as two semicircles:

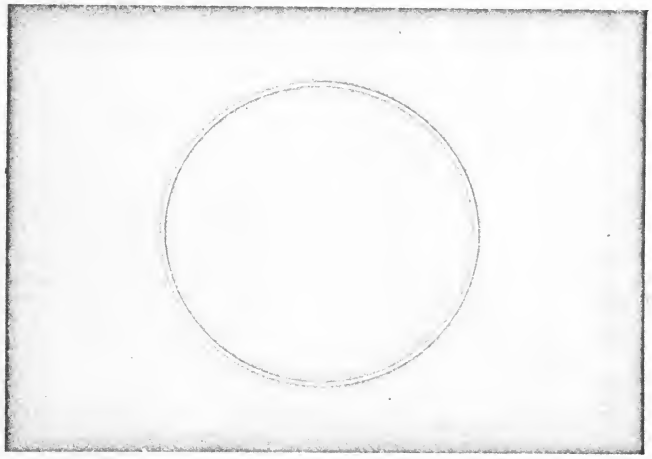

Figure 3—Circle drawn as two semicircles

$$X = \frac{-t+t^2}{0.5-t+t^2}, \quad Y = \frac{0.5-t}{0.5-t+t^2} \tag{6}$$

and

$$X = \frac{t-t^2}{0.5-t+t^2}, \quad Y = \frac{0.5-t}{0.5-t+t^2}$$

The hyperbola was drawn in two segments:

*Xc and Yc are 11-bit decoders.

**The voltage S scales the entire picture and has been dropped from these and succeeding equations.

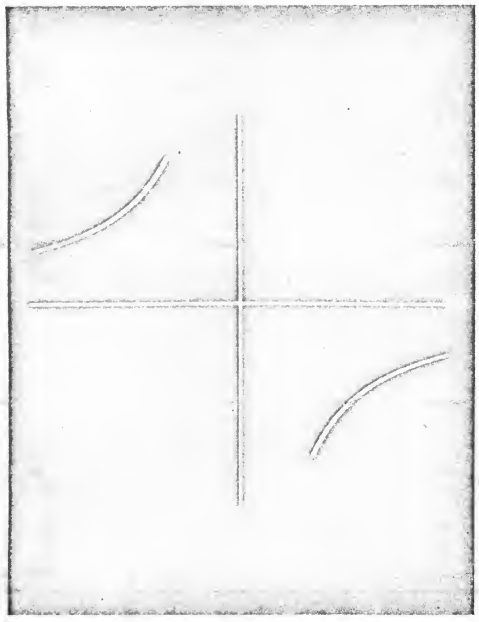

Figure 4—Hyperbolic segments and coordinate axes

$$X = \frac{0.25+t+t^2}{0.5+t}, \quad Y = \frac{1}{0.5+t}$$

and (7)

$$X = \frac{-0.25-t-t^2}{0.5+t}, \quad Y = \frac{-1}{0.5+t}$$

In both figures the range of t was 0 to 1 so that for the semicircles, $0.25 \leq w(t) \leq 0.5$, and for the hyperbola, $0.5 \leqq w(t) \leqq 1.5$. The clock rate was 1 MHz resulting in a 1 ms drawing time for each segment. The scale setting voltage S was set at 4 volts, which corresponds to a radius of 0.5 screen diameters. In order to draw more of a conic in one segment, the minimum value of w(t) must be allowed to get smaller. Since $r = \frac{S}{w(t)}$ the scale setting voltage must be made correspondingly lower in order not to saturate the amplifiers producing r. The signal-to-noise ratio varies directly, however, with the scale setting voltage S resulting in a tradeoff between length of conic segment and S/N. This is illustrated in Figure 5 where an elliptical segment is drawn with $w(t) = 0.28 - t + t^2$. (The x's and y's are the same for the semicircle above.) The minimum value of w(t) is 0.03 occurring at $t = 0.5$, and a maximum is 0.28 occurring at $t = 0$ and $t = 1$. The scale setting for this segment was reduced to $\frac{1}{2}$ volt to prevent saturation. The increased noisiness is apparent as is the variation in beam velocity.

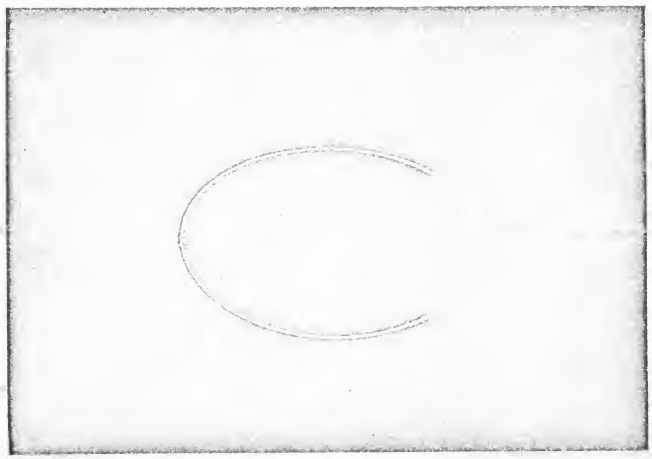

Figure 5—Elliptic segment

The data word format includes two 11-bit subwords for the decoder constants, four N bits which determine the t counter's maximum count, a preset bit described below, and 3 control bits for steering the 10- or 11-bit subwords to the proper buffer registers. These "destination" bits also determine which presets are to be made. Another bit is provided which tells the generator whether it should start or wait for more data. The N bits have meaning only for the data transfer immediately preceding the start of a segment.

In order to draw a curve segment the generator requires in the most general case 11 subwords (nine 10-bit and two 11-bit). However, in many cases of real interest only a few or even one subword has to be changed in going from one segment to another. An example is the generation of similar parallel segments. In this case a translation only is involved and one data transfer (Xc, Yc) is required. To facilitate the drawing of certain common curves a number of presets are provided in the control. Their use obviates a number of data transfers. For example, a preset for drawing lines sets x_2 y_2, w_1, and w_2 to zero and $w_0 = 1$. This preset occurs when the preset bit is a 1 and the destination code for (x_1, y_1) is given.

The multiplying decoder

The basic component of the conic generator is the multiplying decoder shown in Figure 6. Its operation is as follows: A positive analog signal, applied to the driving operational amplifier is inverted, offset, and applied to the resistor-diode network in the input path of the output operational amplifier. Digital levels, applied to diodes D'_0-D'_9 either divert the resistor currents or allow them to flow into the summing node which is kept at virtual ground by the output opera-

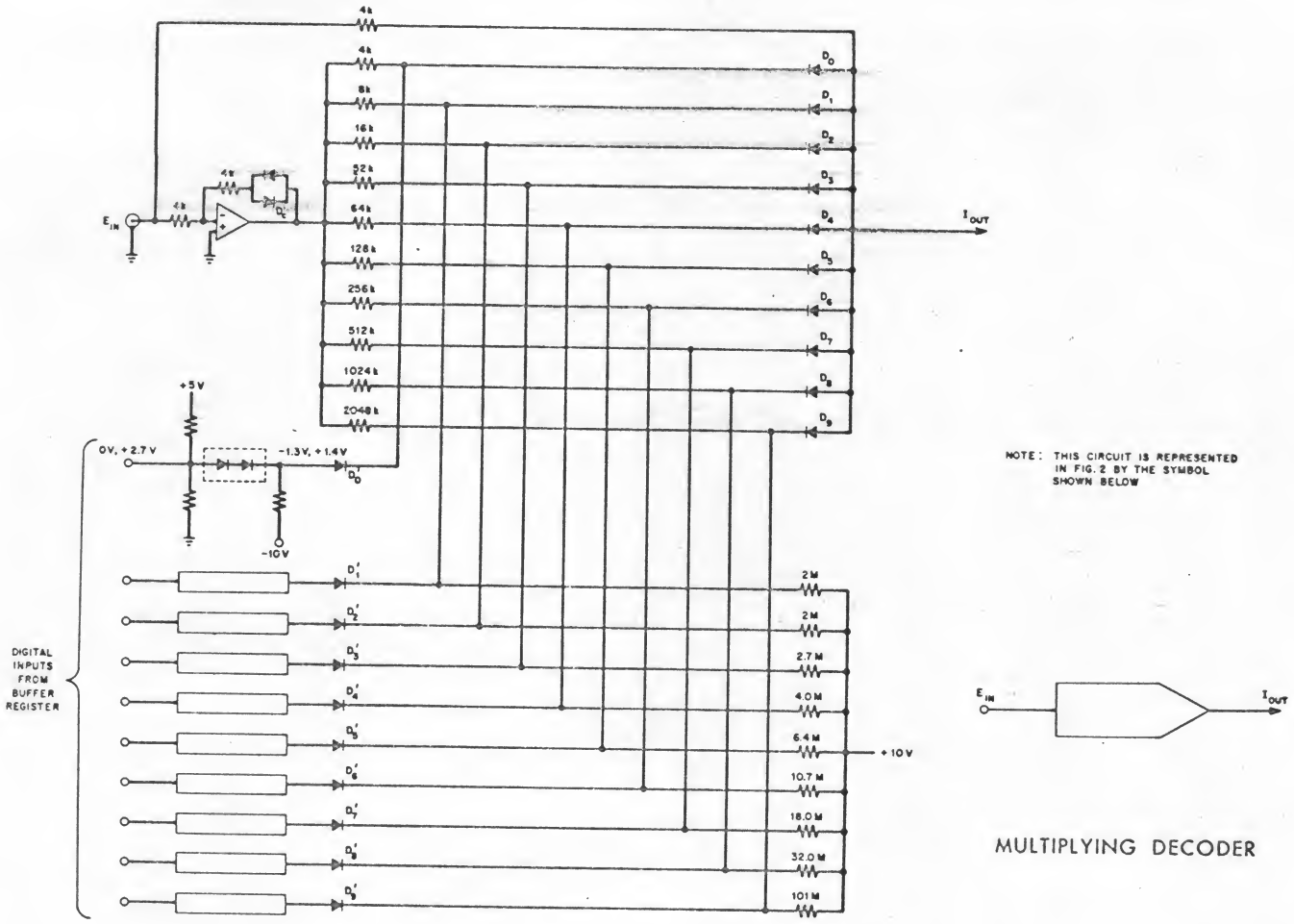

Figure 6—Multiplying decoder. Schematic diagram (output amplifier not shown)

tional amplifier. The summed currents flow through the feedback resistor of the output amplifier by the usual operational amplifier action, developing the output voltage. The currents of several resistor diode networks and their associated driving amplifiers may be summed at a single output amplifier node (see Figure 2). The resistor feeding forward from the input to the summing node of the output amplifier serves to bias the output negatively, allowing outputs of both polarities:

$$E_{out} = E_{in}\left[-1 + \sum_{i=0}^{9}\left(\frac{c_i}{2_i}\right)\right] \tag{8}$$

$c_i = 1$ for an "on" bit

$= 0$ for an "off" bit

Positive input voltages are thereby multiplied over the range (−1.000, +0.999). The level shifting networks preceding the steering diodes D'_0 through D'_9 are designed to be driven from cascode type micrologic outputs. The pertinent characteristics of the operational amplifiers are given in Table 1.

TABLE 1

DC gain	86 dB
Small signal BW (unity gain inverting)	10 MHz
Slewing rate	100 V/μs
Input impedance (open loop)	0.5 MΩ
Output impedance (open loop)	0.5 KΩ
Output voltage	±10 volts
Output current	±30 mA

Each multiplying decoder is packaged on two 4" X 4" circuit cards, and two amplifiers occupying a single card.

Static error

Assume that all the diodes D_e and D_o through

D_9 are identical and have the V-I characteristic $i=I_s(\exp[-v/k]-1)$ over the range of interest, and further that the amplifiers have zero output impedance and infinite input impedance. Referring to Figure 7, where the most significant bit only is shown, the diode D_o in the feedback path of the driving amplifier provides exact compensation for the voltage drop in diode D_o:

$$E_A = -(I_{in}R + V_{DC}) = -(E_{in} + V_{DC}) \quad (9)$$

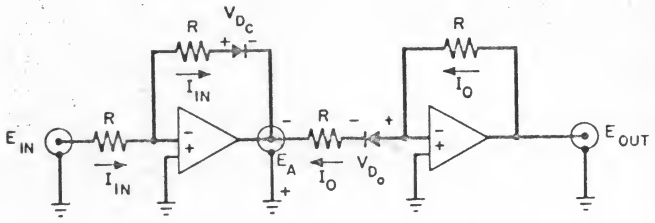

Figure 7—Simplified diagram of multiplying decoder showing most significant bit and output amplifier

But, this is precisely the voltage required to cause I_{in} to flow in D_o; hence in the feedback resistor of the output amplifier. Thus, $E_{out} = I_{in}R = E_{in}$ for all E_{in}. The diode drops in the succeeding lower order bits are only approximately cancelled out by the drop in D_c because their currents (when they are conducting) are less than I_o i.e. $\frac{I_o}{2}, \frac{I_o}{4}, \frac{I_o}{8}, \ldots$ This results in an error in the current, contributed to the summing node by all other active bits. The correct current for the i^{th} leg is:

$$I_i = \frac{E_{in}}{2^iR}$$

and the actual current $\frac{E_{in}+(i)(k)}{2^iR} = \frac{E_{in}}{2^iR} + \frac{ik}{2^iR}$

where k is the exponential factor in the diode equation. If a current source of strength $\frac{-ik}{2^iR}$ were connected to the i^{th} node, the current contribution from that bit when it is "on" would be $\frac{E_{in}}{2^iR} + \frac{ik}{2^iR} - \frac{ik}{2^iR} = \frac{E_{in}}{2^iR}$, the correct value. Note that the excess current term is independent of the input voltage so that in Figure 6, the resistors connected to the 10-volt source supply the compensating current for each node. The additional diode shunting D_c in the feedback path of the driving amplifier keeps the output from drifting into positive saturation, thereby opening the feedback loop. In normal operation it has no effect.

All computing resistors down to and including the fifth most significant bit are low temperature coefficient, thick film resistors; others are evaporated metal film. Diodes D_c, D_o, D_1, and D_2 are a quad, matched to within 3 mV over the operating current range. Diodes D_3, D_4, D_5 are 1N4153 diodes selected for low voltage drop, and the D_6, D_7, D_8, and D_9 are unselected diodes of the same type. The steering diodes D'_o through D'_9 are unselected 1N4153's. The points for the dc error curve in Figure 8 were obtained for three levels of analog input by turning on in succession each bit of a typical decoder and measuring the output voltage. The error in each case is the variation from the nominal output.

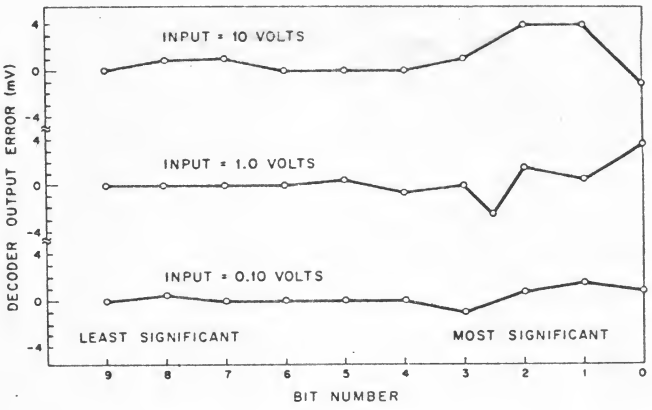

Figure 8—Static error curve of a typical decoder

The effect of the compensating current sources is shown graphically in the photographs of Figure 9. The top photograph shows the ramp output of a t decoder driven by the t counter with constant voltage applied at the analog input terminal. The bottom photograph shows the same output with the compensating sources turned off.

Dynamic characteristics

High speed accuracy of the multiplying decoder for constant digital input is limited by the bandwidth and settling time of the two operational amplifier cascade. Figure 10 shows the small signal frequency response of a multiplying decoder. The input signal was 1 volt peak to peak on a +3 volt bias. The 3db point is 4 MHz. Wide bandwidth is necessary for accuracy at high drawing rates. A high slewing rate capability is required to initiate new conditions at the start of a new curve segment. Dynamic accuracy for changing

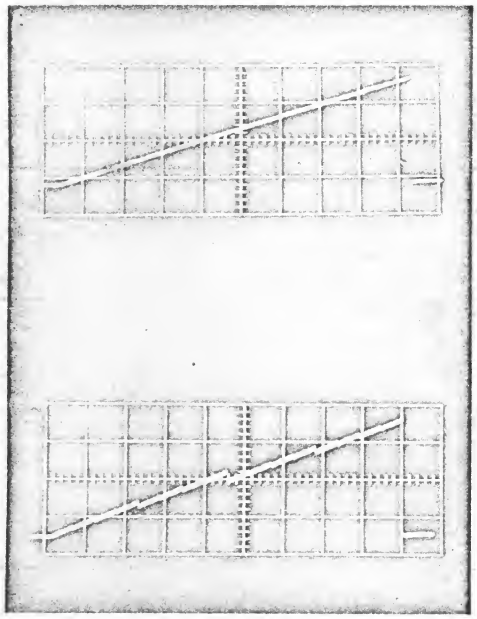

Figure 9—Ramp output of a t decoder with constant input with (a) compensating source on, and (b) compensating source off. 0.1 v/, 1ms/cm.

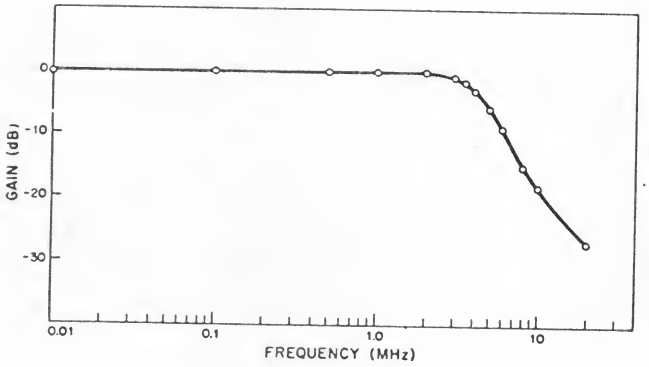

Figure 10—Frequency response of multiplying decoder.

digital inputs is limited by noise generated during switching intervals. Figure 11 shows the switching noise at the output of a t decoder for analog inputs of 1 and 8 volts when the most significant bit is switching. The noise is relatively independent of input amplitude and decreases to 0.1% of full scale in less than 1 μs. The t-decoders are identical to the other decoders. In the generator, switching noise is a limitation only in the t-decoders which switch at the counting rate. The other decoders switch once every curve segment.

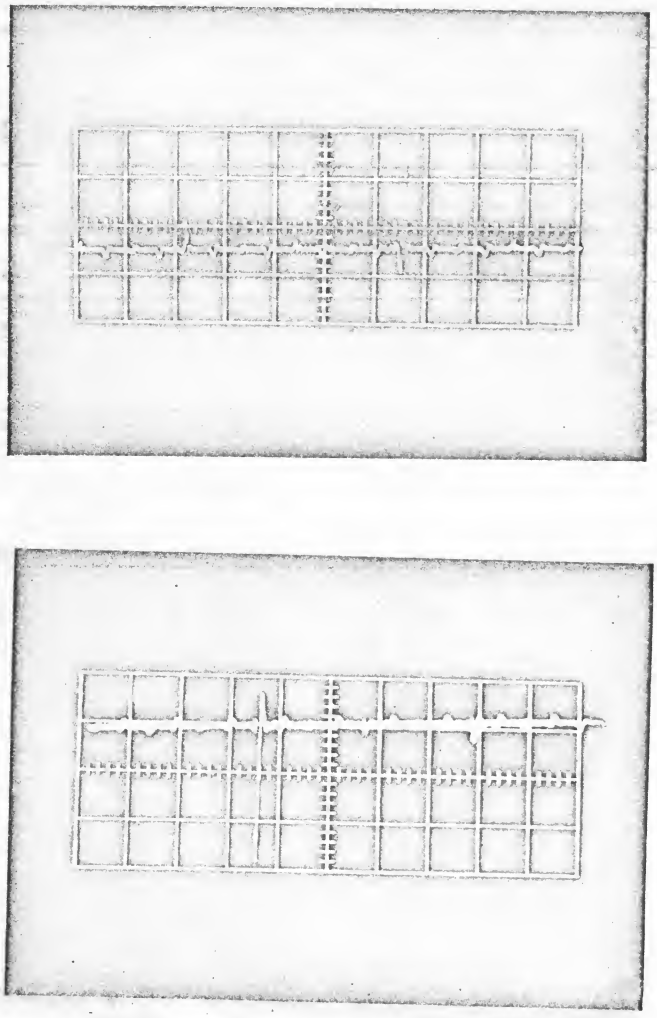

Figure 11—Output of t-decoder showing transient occurring when most significant bit switches, 0.5v/cm, 1μs/cm, (a) 1-volt analog input to decoder, and (b) 8-volt analog input.

The 4k decoder impedance level was chosen to maximize bandwidth and still keep within the output current limitations of the amplifiers. In several locations amplifier outputs were shifted from symmetrical ± 10 volt swings to 0 to -20 volt or 0 to $+20$ volt swings to increase the effective system signal level. In these cases current booster stages were also added to the amplifiers within their respective feedback loops.

Conic generator characteristics

Static accuracy

In Figure 12 the dividing loop is redrawn as an amplifier (or regulator) with linear but time varying feedback. The static error in r, that is its dc or low frequency deviation from the programmed value, depends on the loop gain in the usual manner:

$$r = \frac{S\frac{1}{w(t)}}{1+\frac{1}{\frac{1}{1000\ w(t)}}} \qquad (10)$$

The fractional error $\frac{1}{1000\ w(t)}$ is a maximum when $w(t)$ is a minimum. Thus, over the range $0.25 \leq w(t) \leq 3$ the error varies from 0.4% to 0.03%. Generator accuracy was measured at the output terminals at dc with a DVM for $w(t) = 1$. Each of eight points over X—Y deflection field was programmed 12 different ways, i.e., using different combinations of the w's, x's, and y's giving the same nominal point with the counter stopped. The maximum deviation from the programmed value was ±0.15% of full scale.

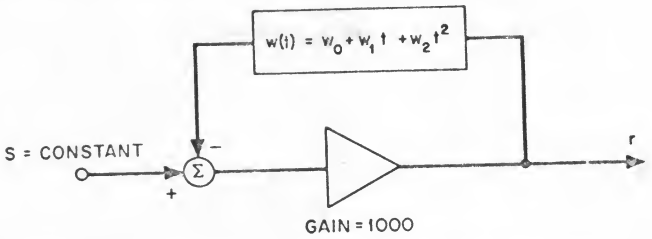

Figure 12—Conic generator dividing loop drawn as a regulator with linear but time-varying feedback.

Stability and high-speed accuracy

The large loop gains required to reduce static errors to tolerable levels would render the dividing loop unstable without frequency compensation. The single lag network shown in Figure 2 insures stability for all positive values of $w(t) \leq 3$. For $w(t) = 3$, the maximum possible value, the gain margin is 6dB and the phase margin 60°. In addition to the static error, the small signal dynamics (i.e., the ability of the dividing loop to correctly produce r(t) at high clock rates) also depend on the value of w(t) and therefore in general vary during the course of generating a segment. The dynamics of the dividing loop for any value of w(t) may be examined (at least approximately) by the artifice of stopping the counter and injecting a signal at the summing node of the t-decoder input amplifier and examining the resultant signal fed around to r. Table 2 gives the results of such a study for a step input. The responses vary from overdamped with risetime 2 μs for $w = 0.25$ to underdamped with risetime 250 ns, natural frequency 2 MHz, and damping constant 0.3 at $w = 3$. The risetimes are a measure of the delay the signal r will experience. For the smaller values of w the single lag network dominates the response. This is essentially a "velocity" error in contrast to the "position" error discussed above in the section on static error. The response of the loop in drawing a curve where there is a substantial variation in w(t) may be approximated by several piecewise calculations using the proper dynamics for each section. As an example, consider $w(t) = 0.25 + t + t^2$, $0 \leq t \leq 1$. If we break the time interval into three zones centered at $t = 0.2$, 0.5, and 0.8, we find that r experiences delays of 440 ns, 260 ns, and 150 ns.

Speed limitations

The curve drawing speed is presently limited by the noise generated in the t decoders during switching. At high rates the smeared out t-decoder spikes are noticeable. This limits the speed of curve segment generation to about 1 ms across the screen and 200 μs full scale for straight line segments. Since the switching noise is essentially independent of signal level, an increase in signal from its relatively low level (±10 volt decoder outputs) should result in a corresponding increase in S/N with attendent increased speed capabilities.

TABLE 2

w_0	w_1	w_2		Natural Frequency	Risetime 10%-90%	Damping Constant
1	1	1	Under Damped	2 MHz	250 ns	0.3
0.75	0.75	0.75	Under Damped	1.5 MHz	350 ns	0.6
1	1	0	Under Damped	1 MHz	350 ns	0.8
1	0	1	Under Damped	1 MHz	350 ns	0.7
0	1	1	Under Damped	1 MHz	350 ns	0.7
0	1	0	Critically Damped		600 ns	
0	0.5	0	Over Damped		1 μs	
0	0.25	0	Over Damped		2 μs	

SUMMARY

The present limit on drawing speed is set by the t-decoder switching noise rather than the bandwidth of the dividing loop and multipliers external to the loop. It should be possible to raise the limit almost in proportion to any increase in signal level, provided that decoder amplifier bandwidth is not seriously reduced in going to a higher signal level. Extension to cubics using the same techniques should be straightforward, although the additional phase lag introduced by the t^3 decoder would probably result in a slight decrease in

loop speed in order to maintain adequate stability margins.

The limitation of the range of w(t) due to amplifier saturation does not appear to require that large numbers of segments be pieced together to form curves, but this matter is still under study.

The limitation on accuracy imposed by the variation in w(t) in Equation 10 may be eliminated by introducing a compensating circuit to keep the loop gain constant by varying amplifier gain to track w(t).

ACKNOWLEDGMENT

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